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09/710,606	11/10/2000	Jong-Myoung Lee	AB-1060 US	5064

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EXAMINER	
PAREKH, NITIN	
ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 05/08/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Acti n Summary	Application N .	Applicant(s)	
	09/710,606	LEE, JONG-MYOUNG	
	Examiner	Art Unit	
	Nitin Parekh	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 March 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2,4 and 8-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2,4 and 8-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 November 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Request for Continued Examination

1. A request for continued examination (RCE) under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 03/21/03 has been entered. An action on the RCE follows.

2. The amendment filed on 01/21/2003 has been entered.

Drawings

3. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims.

Claim 11, line 2 cite: ".... the bonding pads are arranged in two parallel rows".

Claim 12, line 2 cite: ".... the parallel rows are arranged....".

Therefore, two parallel rows must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim R jections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 2 and 8-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Iwaya et al. (US Pat. 6392295) in view of Ohi et al. (US Pat. 5235207).

Regarding claim 8, Iwaya et al. disclose a Lead-on-chip (LOC) semiconductor package comprising:

- a semiconductor chip (1 in Fig. 1 and 2) having a chip periphery and a plurality of bonding pads (1a in Fig. 1), the bonding pads being within the chip periphery in a single row, the row being centered and arranged in a generally longitudinal direction on the chip (Fig. 1)
- a plurality of general leads (2b in Fig. 1 and 2), the general leads having inner and outer portions (not numerically referenced in Fig. 1 and 2; see lead portions inside/outside a sealing resin 4 in Fig. 1 and 2), the inner portions being spaced from and not crossing the chip periphery (see 2b in Fig. 1 and 2)

- a first plurality of wires (3 in Fig. 1 and 2) extending between the corresponding bonding pads and the inner portions of the general leads, thereby extending across the chip periphery
- a plurality of support/stable leads (2a in Fig. 1 and 2) including a total of fifty leads (Col. 5, line 42), each lead having inner and outer portions, the inner portions having an attachment section /contact portion having an adhesive composition (not numerically referenced in Fig. 1 and 2; see Col. 5, line 40) between the chip and the inner portion of each of the support/stable leads providing functions of the chip support and the package stability
- a second plurality of wires (3 in Fig. 1 and 2) within the chip periphery extending between the corresponding bonding pads and the inner portions of the support/stable (see Fig. 1), and
- a molding resin (4 in Fig. 1 and 2) encapsulating the chip, the inner portions of the support/stable leads and the general leads, the adhesive composition and the first and second plurality of wires

(Fig. 1-8; Col. 5, line 5- Col. 7, line 50).

Iwaya et al. fail to teach the inner portions of the support/stable leads being in a generally planar relationship with those of the general leads.

Ohi et al. teach using a LOC device where an inner portion of common/stable lead is in a generally planar relationship/flush with that of the general/signal lead

(2A1 and 4A respectively in Fig. 9) so that the lead frame manufacturing can be simplified (Col. 9, line 47).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the inner portions of the stable leads being in a generally planar relationship with those of the general leads as taught by Ohi et al. so that the lead frame manufacturing can be simplified and the yield can be improved in Iwaya et al's package.

Regarding claim 2, Iwaya et al. teach the outer portions of the support/stable leads and general leads being extended from the molding resin (see outer portions of 2a and 2b and resin 4 in Fig. 1 and 2) (Col. 7, line 5-10).

Regarding claim 9, Iwaya et al. teach the plurality of bonding pads (1a in Fig. 1) being arranged in the single row (Col. 5, line 34).

Regarding claim 10, Iwaya et al. teach the single row being generally centered and arranged in a generally longitudinal direction on the chip (Fig. 1; Col. 5, line 25-48).

6. Claims 11 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Iwaya et al. (US Pat. 6392295) and Ohi et al. (US Pat. 5235207) as applied to claim 8 above, and in further view of Russell (US Pat. 5545920).

Regarding claim 11, Iwaya et al. and Ohi et al. teach substantially the entire claimed structure as applied to claim 8 above, except the plurality of bonding pads being arranged in two parallel rows.

Russell teaches a LOC package having a variety of bonding pad configurations on a chip/component including an arrangement having two parallel rows (see rows 121 in Fig. 6; Col. 4, line 50-55).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the bonding pads being arranged in two parallel rows as taught by Russell so that wire bond repair capability can be improved and the longitudinal dimension of the chip can be reduced in Iwaya et al. and Ohi et al's package.

Regarding claim 12, Iwaya et al. and Ohi et al. teach substantially the entire claimed structure as applied to claims 8 and 11 above, except the parallel rows being arranged in a generally longitudinal direction about a central longitudinal axis of the chip.

Russell teaches a LOC package having a variety of bonding pad configurations on a chip/component including an arrangement having two parallel rows, the rows being arranged in a generally longitudinal direction about a central longitudinal axis of the chip (see rows 121 in Fig. 6; Col. 4, line 50-55).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the bonding pads being arranged in two parallel rows as taught by Russell so that wire bond repair capability can be improved and the longitudinal dimension of the chip can be reduced in Iwaya et al. and Ohi et al's package.

7. Claims 4 and 13-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Iwaya et al. (US Pat. 6392295) and Ohi et al. (US Pat. 5235207) as applied to claim 8 above, and in further view of Takeuchi (US Pat. 5977614).

Regarding claim 13, Iwaya et al. and Ohi et al. teach substantially the entire claimed structure as applied to claim 8 above, except the attachment sections of the support/stable leads being configured to increase the bond strength between the attachment section and the adhesive composition.

Takeuchi teaches a LOC package having a configuration of support/stable leads (35a/35b in Fig. 6) where the leads are patterned having a shape of a maze/serpentine having an increased surface area at the tip portions providing increased bonding area so that the thermal stress and wire bonding defects in the resin sealed package are reduced (Col. 8, line 22-26; Col. 8, line 15-19).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the support/stable leads being configured to increase

the bond strength between the attachment section and the adhesive composition as taught by Takeuchi so that the thermal stress can be reduced and wire bonding yield can be improved in Iwaya et al. and Ohi et al's package.

Regarding claim 4, Iwaya et al. and Ohi et al. teach substantially the entire claimed structure as applied to claim 8 above, except the attachment section of the stable leads including a substantially greater width than that of an adjacent inner portion.

Takeuchi teaches a LOC package having a configuration of support/stable leads (35a/35b in Fig. 6) where the attachment section of the respective leads has a substantially greater width (see 36a in Fig. 6) and an increased surface area than an adjacent inner portion (Col. 7, line 30-Col. 8, line 26).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the attachment section of the stable leads including a substantially greater width than that of an adjacent inner portion as taught by Takeuchi so that the thermal stress can be reduced and bonding surface area can be increased in Iwaya et al. and Ohi et al's package.

Regarding claim 14, Iwaya et al. and Ohi et al. teach substantially the entire claimed structure as applied to claim 8 above, except the support/stable leads having a serpentine configuration.

Takeuchi teaches a LOC package having a configuration of support/stable leads (35a/35b in Fig. 6) where the leads are patterned having a shape of a maze/serpentine and having an increased surface area at the tip portions providing increased bonding area so that the thermal stress and wire bonding defects in the resin sealed package are reduced (Col. 8, line 22-26; Col. 8, line 15-19).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the support/stable leads having a serpentine configuration as taught by Takeuchi so that the thermal stress can be reduced and wire bonding yield can be improved in Iwaya et al. and Ohi et al's package.

Regarding claim 15, Iwaya et al., Ohi et al. and Takeuchi teach substantially the entire claimed structure as applied to claims 8 and 13 above, except the attachment sections of the support/stable leads being configured to form an open structure having an inside edge and an outside edge.

Ohi et al. further teach a LOC package having a variety of configurations of attachment sections/inner portions of the common/stable leads (2A in Fig. 11d and 11i) where the leads are configured to form an open structure having an inside edge and an outside edge (Col. 9, line 48-55).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the attachment sections of the support/stable leads being configured to form an open structure having an inside edge and an outside edge

as taught by Ohi et al so that the thermal stress can be reduced and the bonding area can be increased in Iwaya et al. and Takeuchi's package.

Response to Arguments

9. Applicant's arguments with respect to claims 2, 4 and 8-15 have been considered but are moot in view of the new ground(s) of rejection.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin Parekh whose telephone number is 703-305-3410. The examiner can normally be reached on 09:00AM-05:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 703-308-2772. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722, 703-308-7724 or 703-872-9318 (Right FAX) for regular communications; 703-872-9310 (Right FAX) for After Final communications and 703-872-9310 (Right FAX) for customer service.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-306-3431.

Nitin Parekh

NP

05-02-03

Tom Thomas

TOM THOMAS
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